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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,387	04/14/2004	William Bradley Vest	174/300	8458

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EXAMINER	
TRAN, ANH Q	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 07/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/825,387	VEST ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28,29 and 31* is/are allowed.

6)☒ Claim(s) *1,2,4,7-10,12-27 and 30* is/are rejected.

7)☒ Claim(s) *3,5,6 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/14/04*. (7-19-05)
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4, 7-10, 12-17, 22, 27 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Agrawal et al (5,740,069).

Agrawal shows:

1. A programmable logic device comprising:

a plurality of logic elements (CLB) for performing logic functions that are arranged in one or more logic array blocks (Fig. 1);

at least one input/output (I/0) block (96, Fig. 60) for passing signals between said LEs and one or more I/0 pads (4500, Fig. 45 and 4600, Fig. 46) associated with said I/0 block, said I/0 pads providing input and output to said programmable logic device; and

a signal routing architecture (switch matrix, segment box, and PIP, Figs. 8-10) for routing signals among said LEs and said at least one I/0 block comprising:

a plurality of horizontal and vertical signal routing conductors (Figs. 4-5) and drive circuitry (Fig. 20);

at least one block input multiplexer (4501, Fig. 45 and 4600, Fig. 46) for selectively providing signals from said plurality of horizontal and vertical signal routing conductors to said at least one I/0 block; and

at least one output bypass path for providing a direct connection (Fig. 53-55) between an output from one of said plurality of LEs and said at least one I/0 block.

2. The programmable logic device of claim 1 wherein said at least one output bypass path is used for routing a data signal (data output from X3, and data input from FN4).

4. The programmable logic device of claim 1 wherein said at least one output bypass path is used for routing signals to an I/0 register (4634, Fig. 46).

7. The programmable logic device of claim 1 wherein said at least one I/0 block comprises at least one I/0 multiplexer, said output bypass path being coupled to one of the inputs of said at least one 1/0 multiplexer (col. 28, lines 36-39 and col. 31, lines 5-9).

8. The programmable logic device of claim 7 wherein said at least one block further comprises at least one output buffer (4506, Fig. 45 and 4642, Fig. 46), the output of said at least one I/0 multiplexer being coupled through said output buffer to one of said I/0 pads.

9. The programmable logic device of claim 7 wherein said at least one I/0 block further comprises one or more I/0 registers (4615 & 4634, Fig. 46).

10. The programmable logic device of claim 7 wherein said at least one I/0 block further comprises one or more output enable multiplexers (4337, 4639, 4648).

12. The programmable logic device of claim 1 wherein said LABS are arranged in a one dimensional array.

13. The programmable logic device of claim wherein said LABs are arranged in a two dimensional array (two CLBs either in a row or column considered a LAB).

14. The programmable logic device of claim 1 wherein said drive circuitry comprises a driver input multiplexer (2, Fig. 18) and a driver (2001, 2003 and 2004 Fig. 20).

15. The programmable logic device of claim 15 wherein said drive circuitry comprises a buffer (2001) and one (2004) or more programmable switches.

16. The programmable logic device of claim 15 wherein said one or more programmable switches are pass transistors (2004, Fig. 20).

17. the limitations are rejected as above claims 14-16.

22. An integrated circuit device (Fig. 1) comprising the programmable logic device of claim 1.

27. the limitations of claim 27 are rejected as above claim 1.

30. the apparatus described above is applicable to the method claim 30.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 18-21, 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al (5,740,069) in view of Schlecher et al (6,366,120).

Agrawal discloses the claimed invention except for memory circuitry, processing circuitry coupled to programmable logic device of claim 1 mounted on the printed circuit board. Schleicher discloses the memory circuitry, the processing circuitry coupled to programmable logic device of claim 1 mounted on the printed circuit board (Fig. 9). It

would have been obvious to one having ordinary skill in the art at the time the invention was made to provide programmable logic device of claim 1 with the memory circuitry and the processing circuitry coupled to the bus system mounted on the printed circuit board, in order to provide a wide variety of applications where the advantage of using programmable or reprogrammable logic is desirable.

Allowable Subject Matter

5. Claims 3, 5-6, 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 28-29, and 31 are allowed.

7. The following is an examiner's statement of reasons for allowance: with respect to claims 29 and 31, in addition to other limitations in the claims, the prior fails to teach or disclose the applicant's invention as claimed, particularly the feature describing at least one input bypass path for providing a direct connection between the at least one I/O block to one or more of the plurality of segmented routing conductors.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

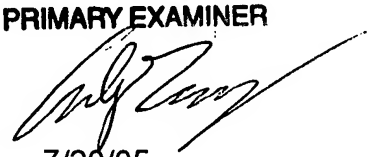
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER



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